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SUBJ: PRODUCT DESCRIPTION

CC: C. M. Shuler
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S-70021-B 9500 Processor (Type 3016)

The attached subject Product Description, ("PRELIMINARY" information only), is submitted for your review and/or information. Comments are requested in this office no later than fifteen (15) days from the above transmission date. Comment directly on this sheet if desired and note that "No Comments" or "No Interest" is a valid comment.

The Product Description may be kept for your files.

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MWB/dll

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C. M. Shuler

PRELIMINARY ISSUE
COMPANY CONFIDENTIAL

UNIVAC
DIVISION OF SPERRY RAND CORPORATION
DATA PROCESSING DIVISION

Number: S-70021

PRODUCT DESCRIPTION

Date Approved:

Product Code: 251	System Code:	Rev. Date 5-13-66	Rev. B

Product Title & Type Number:

9500 Processor (Type 3016)

Performance Objectives:

Provide a general purpose, high-speed central processor which effectively utilizes a 16 bit data width. Design emphasis is to be on a medium scale processor having real-time, batch and scientific computing capability. I/O design will be consistent with maintaining adequate thruput to accomplish these objectives.

Abstract:

This product description contains functional specifications for a low-to-medium cost Processor. One Multiplexer channel is provided for connecting up to eight control units to the Processor. Four optional Selector I/O channels are provided for high speed peripheral data transfer. Floating Point arithmetic and Decimal arithmetic are also optional.

Revision																						
	Rev.	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	Page No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
	Rev.	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	Page No.	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

Related Specifications & Standards:

P-10046 I/O Interface
P-20050, Rev. D Environmental
S-70020 9500 System
S-70022 9500 Working Storage
S-70023 Operator's Console

Notes, Unusual Requirements, Unique Features:

Prepared By: Systems Design | Date: 10-6-65 | UPS 5-20-66 | 5-20-66

Group Manager Date,	Director of Engineering Date	Manager, Technical Staff Date
Vice President - Marketing Manager of Products Date		

PRODUCT DESCRIPTION

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1.0 SCOPE

This document describes the 9500 Processor, Type 3016, a medium sized business processor capable of performing real-time, batch, and scientic data processing.

The processor is not intended for use in multiprocessor systems.

Data processing is accomplished in a 16-bit parallel mode using Supervisor, Standard, and the Optional (decimal and floating point) instructions. The Standard and Optional instructions are compatible with those of the IBM* System 360. Control circuitry provides for processing of interrupts, protection of operating programs in memory, and detection of memory parity errors.

The following items are provided as standard equipment with each processor:

- One Multiplexer I/O Channel
- One Operator's Control Console
- One maintenance panel

In addition, up to four Selector I/O Channels are available on an optional basis.

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2.0 FUNCTIONAL CHARACTERISTICS

The 9500 Processor comprises three operational sections; Control, Arithmetic, and Input/Output. Main Storage, although separately housed and powered, functions as an integral part of the processor. As such, those main storage characteristics which are processor functions will be described in this document; all others are described in Product Description S-70022.

2.1 Control Section

The Control Section controls the sequencing of instructions, interprets and controls the execution of each instruction, and initiates the cycling of main storage. In addition, this section handles Interrupts, Error Checking, Storage Protection, and the Supervisor-Standard functions.

2.2 Arithmetic

The Arithmetic Section performs all data manipulations which include; logical and numerical arithmetic, data comparison, data shifting, and single or double indexing of operand addresses. This section contains an Adder which performs the arithmetic in a 2's complement form.

2.3 Input/Output

The Input/Output (I/O) section upon receiving an I/O instruction from the Control Section; initiates, directs, and monitors the transfer of data between Storage and the Peripheral subsystems. The data transfer is performed concurrently with other Processor functions.

The I/O section has up to five I/O channels; one Multiplexer channel and up to four Selector channels. The Selector channels are available on an optional basis and each channel handles only one Standard Subchannel.

The Multiplexer channel can handle up to eight subchannels via the respective controllers.

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2.3.1 Multiplexer Channel

The Multiplexer Channel (Figure 1) is part of the minimum processor configuration. This channel provides for handling both communications and standard controllers (standard peripheral subsystems). The maximum number of controllers is eight; either communications or standard, or a combination of both types. Communications controllers can handle a maximum of 128 devices collectively, standard controllers a maximum of 16 each.

There is one Access Control Register (ACR) for each of the 128 communications devices and one for each of the 8 Standard Subchannels. The ACR's are located in main storage addresses. The individual ACR's provide for concurrent operation of devices. For instance, if two Communications Controllers (two Line Terminal Controllers each with 64 devices) are used, then six is the maximum number of Standard Subchannels allowed. In this configuration 128 communications devices and six standard subchannel devices (one per Controller) can be operated concurrently, all 134 devices can access storage concurrently, and all data is multiplexed.

2.3.2 Selector Channels

Up to four Selector Channels (one shown in Figure 2) are available as options. The four Access Control Registers, one per Selector Channel, are located in the Processor cabinet. Each channel handles Standard Controllers only. Each Selector Channel handles up to eight Controllers with each controller usually having one device but with up to 16 devices possible.

Since each Selector Channel has only one Access Control Register, the controller devices are serviced on a one-at-a-time basis. That is, once the data transfer from any particular device is initiated, that transfer must be completed before any other device can transfer data.

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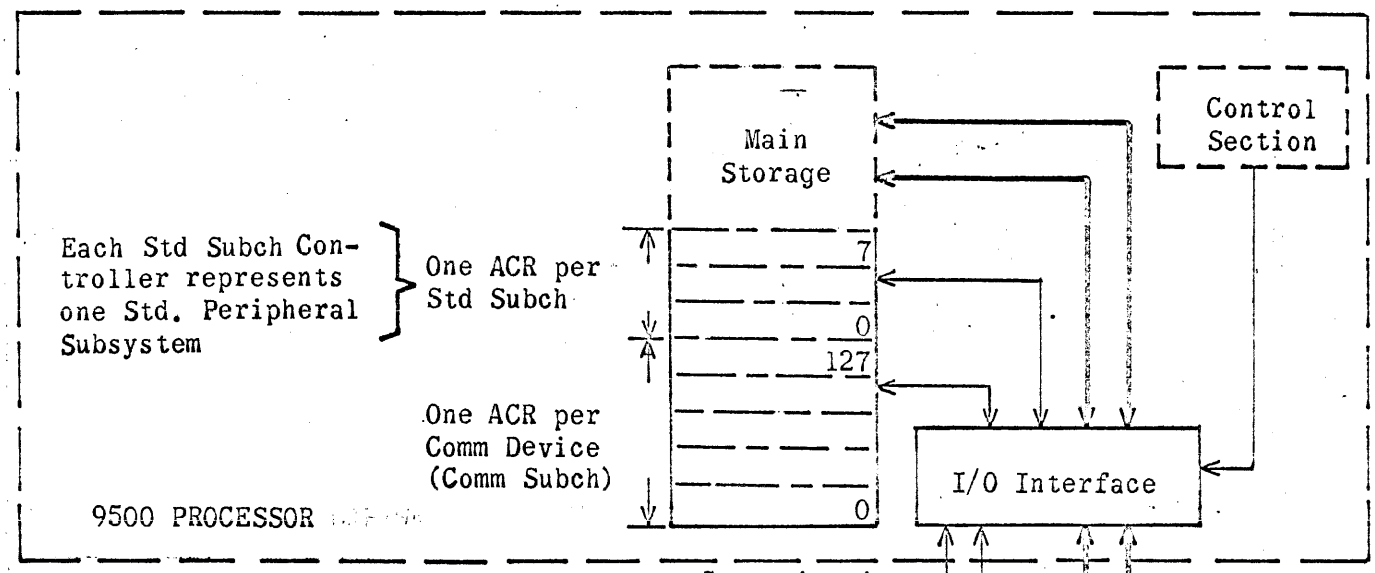
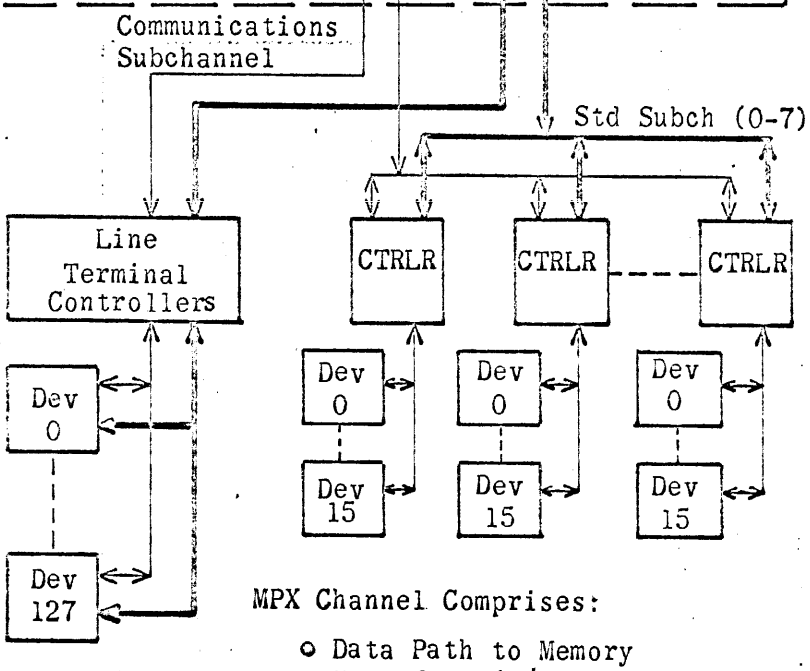


Address Format - ccc tsss uuuu

ccc=000 (selects MPX channel)

tsss for Comm Subch:
t=0 (selects Comm Subch)
sssuuuu= 0 thru 127 (selects Device)

tsss for Std. Subch:
t=1 (selects Std. Subch)
sss= 0 thru 7 (selects CTRLR)
uuuu= 0 thru 15 (selects S/S Device)



Legend:

---- Denotes units are not part of channel

——— Control Lines

——— Data Lines

On Communications Subch - One ACR per Communications Device (up to 128)
On Std. Subch. - One ACR per Controller (Std. Periph. Subsystem)

MPX Channel Comprises:

- Data Path to Memory
- Interface (I/O Control)
- Access Control Registers - Located in Main Storage
- Communications and/or Subchannels

Figure 1. Multiplexer Channel

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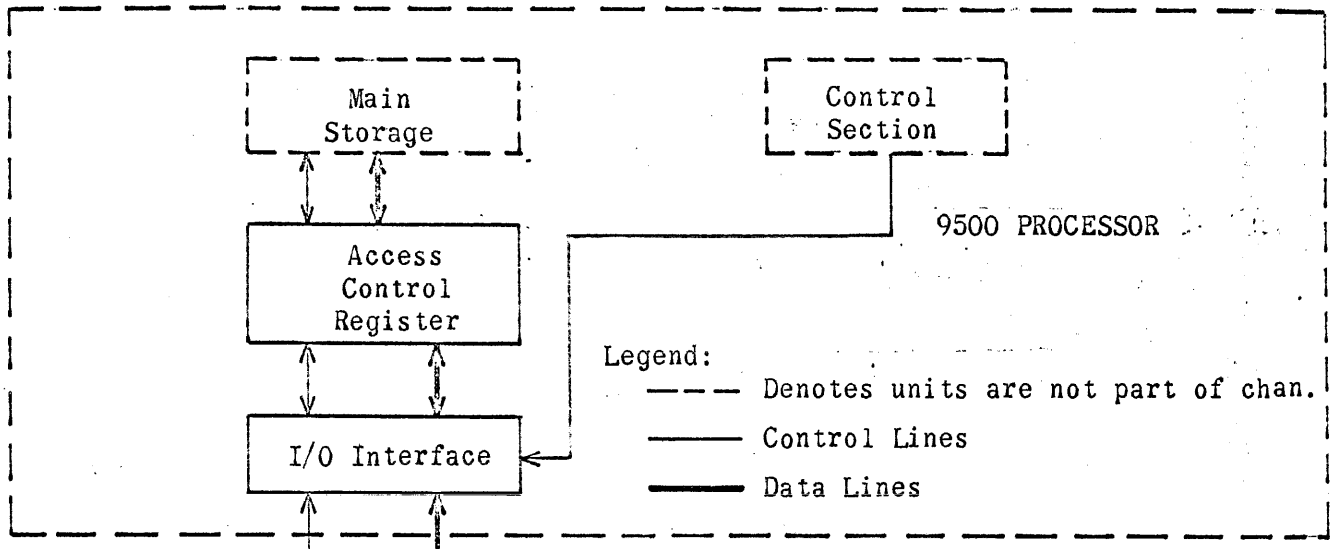

Address Format - ccc tsss uuuu

ccc= 001 - ch 1
010 - ch 2
011 - ch 3
100 - ch 4

t= 0, always

sss= 0 thru 7 (selects CTRLR of a Std Peripheral Subsystem)

uuuu= 0 thru 15 (selects peripheral device)

Each Selector Channel Comprises:

- Data Path to Storage
- One ACR per Channel
- Up to eight Standard Peripheral Subsystems
- Interface (I/O Control)
- One or more devices per Controller, up to 16

Figure 2. Selector Channel

2.3.3 Channel Command Word

The Channel Command Word (CCW) specifies the command to be executed and, for commands initiating I/O operations, it designates the storage area associated with the operation and the action to be taken whenever transfer to or from the area is completed. The CCW's can be located anywhere in main storage, and more than one can be assoicated with a START I/O instruction. The channel refers to a CCW in main storage only once, whereupon the pertinent information is stored in the channel.

The first CCW is read from storage during the execution of START I/O instructions. Each additional CCW in the sequence is obtained when the operation has progressed to the point where the additional CCW is needed. Obtaining the CCW's by the channel does not affect the contents of the location in main storage.

The CCW format is shown in Figure 3.

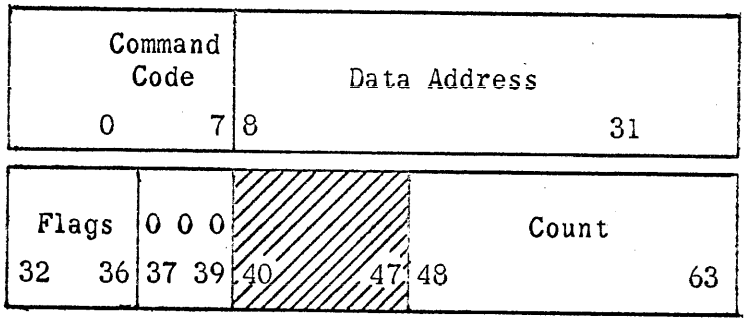

Figure 3. Channel Command Word Format

The fields in the CCW are allocated for the following purposes:

Command Code: Bits 0-7 specify the operation to be performed.

Data Address: Bits 8-31 specify the location of an eight-bit byte in main storage. It is the first location referred to in the area designated by the CCW.

Chain-Data (CD) Flag: Bit 32, when one, specifies chaining of data. It causes the storage area designated by the next CCW to be used with the current operation. When bit 32 is zero, the current control word is the last one for the operation.

Bits 33 and 34 must be zero's.

Skip (SKIP) Flag: Bit 35, when one, specifies suppression of transfer of information to storage during a read, read-backward, or sense operation. When bit 35 is zero, normal transfer of data takes place.

Program-Control-Interruption (PCI) Flag: Bit 36, when one, causes the channel to generate an interrupt condition upon reading the CCW from storage. When bit 36 is zero, normal operation takes place.

Bit positions 37-39 of every CCW other than one specifying transfer in channel must contain zeros.

The contents of bit positions 40-47 of the CCW are ignored.

Count: Bits 48-63 specify the number of eight-bit byte locations in the storage area designated by the CCW.

2.3.4 I/O Interrupts

All Input/Output interrupts will be automatically placed into a Channel Status table in main storage. The table entry will include channel number, device number status, and interrupt class. Tabling will be performed in the following manner. The program will set a pointer register. When a device presents an interrupt, the I/O hardware will access the pointer, store the status, channel number, and device number at that address, increment the pointer and restore it. The first time that the processor is in the proper state to be interrupted by the class of interrupt which occurred, the program will be interrupted. Only one interrupt will occur even if several devices have presented interrupts. To determine how many interrupts have occurred, the pointer must be accessed to determine how many times it has been advanced. The class of the interrupts in the table can be determined by examining the sign of the table entry; negative for class one, positive for class two.

2.3.5 I/O Transfer Rates

The I/O data transfer rates are as follows:

Multiplex (ESI) Channel:

167,000 bytes per second maximum. I/O uses 60% of the available main storage cycles.

Selector Channel:

1,500,000 bytes per second maximum aggregate total for all four channels. I/O uses 50% of the available main storage cycles. 400,000 bytes per second maximum for any one channel.

2.4 Main Storage

2.4.1 Main Storage Characteristics

The main storage data word is 18-bits wide and comprises two 8-bit bytes with one parity bit per byte. Parity for each byte is odd. The format of the data word as it appears on the maintenance panel is shown in Figure 4.

P_M	P_L	Most Significant Data Byte	Least Significant Data Byte

Figure 4. Main Storage Data Word Format

Storage is addressable by byte but both bytes are received whenever a storage word is read. Individual bytes may be written into storage if an instruction requires that this be done.

Main Storage access priority is as follows: Selector channel 1, 2, 3, 4; MPX channel; Control.

See Product Specification S-70022 for other Main Storage characteristics.

2.4.2 Data and Address Boundaries

The bytes of Main Storage are numbered consecutively from 0 through the maximum number of bytes minus one (262,143). Bytes may be addressed separately or in groups. Two consecutive bytes constitute a halfword if the address of the Most Significant Byte (MSB) is divisible by two. Four bytes make a word if the address of the MSB is divisible by four. Eight bytes make a double word if the MSB-Address is divisible by eight. Therefore, definite boundaries exist for all fixed length data fields. Instruction lengths are 2, 4, or 6 bytes and are thereby restricted to halfword boundaries only. Since storage is actually a halfword wide, all fixed boundaries fall between words. Variable length data fields are not restricted by boundaries. All operands are addressed by the position of the most significant byte as are all instructions.

2.4.3 Memory Page-Mapping

Page-Mapping is the division of processor storage into units, called Pages, and then mapping the Actual addresses of the randomly located Pages so that they appear as a single, continuous storage area known as Virtual addresses. Control bits associated with each Page description provide for an automatically controlled program segmentation. This program segmentation reduces storage requirements by storing only those Pages which are currently active. It also makes possible the operation of programs in those processors having various sized increments of available main storage.

The Page-Mapping characteristics are:

- Pages are 512-byte units.
- Page-maps are held in main storage.
- The map pointer allows complete freedom in assigning the locations of program (or task) page maps.
- Relocation is bypassed when appropriate.

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The Address translation process shown in Figure 5 is performed whenever relocating a storage address is required during either a Processor or an I/O storage access. The process is accomplished as follows:

1. Bit positions 14 through 18 of the Virtual Address are combined with bit positions 8 through 12 of the Map Pointer to form the Page Descriptor Address. This address is sent to main storage and a read is initiated.

2. Simultaneously with Step 1, a comparison of the Page Number and the Limit Number is made. This comparison assures memory protection in that the Virtual Address cannot exceed the limits set by the supervisor routine.

3. This half-word read from storage contains the Page Control bits and the Actual Page Address. This address, bits 7 through 15, are prefixed to the Byte Address of the Virtual Address to form the Actual Storage Address. This Actual Storage Address is sent to main storage and a read/write is initiated to obtain the Operand/Instruction Data.

4. Simultaneously with Step 3, the Program Control bits are interrogated to determine the legality of the storage access according to the Page Control bits tabulated on Figure 5.

This Address relocation process is at times bypassed during Processor storage accesses in order to minimize degradation of processor speed. The conditions under which the relocation process is bypassed are as follows:

1. During normal access of Next Instruction (The NI address is held in relocated form and relocation translation occurs only when a page boundary is crossed or a branch occurs).

2. During normal operation of I/O transfer of data (Again relocation translation occurs only when a boundary is crossed).

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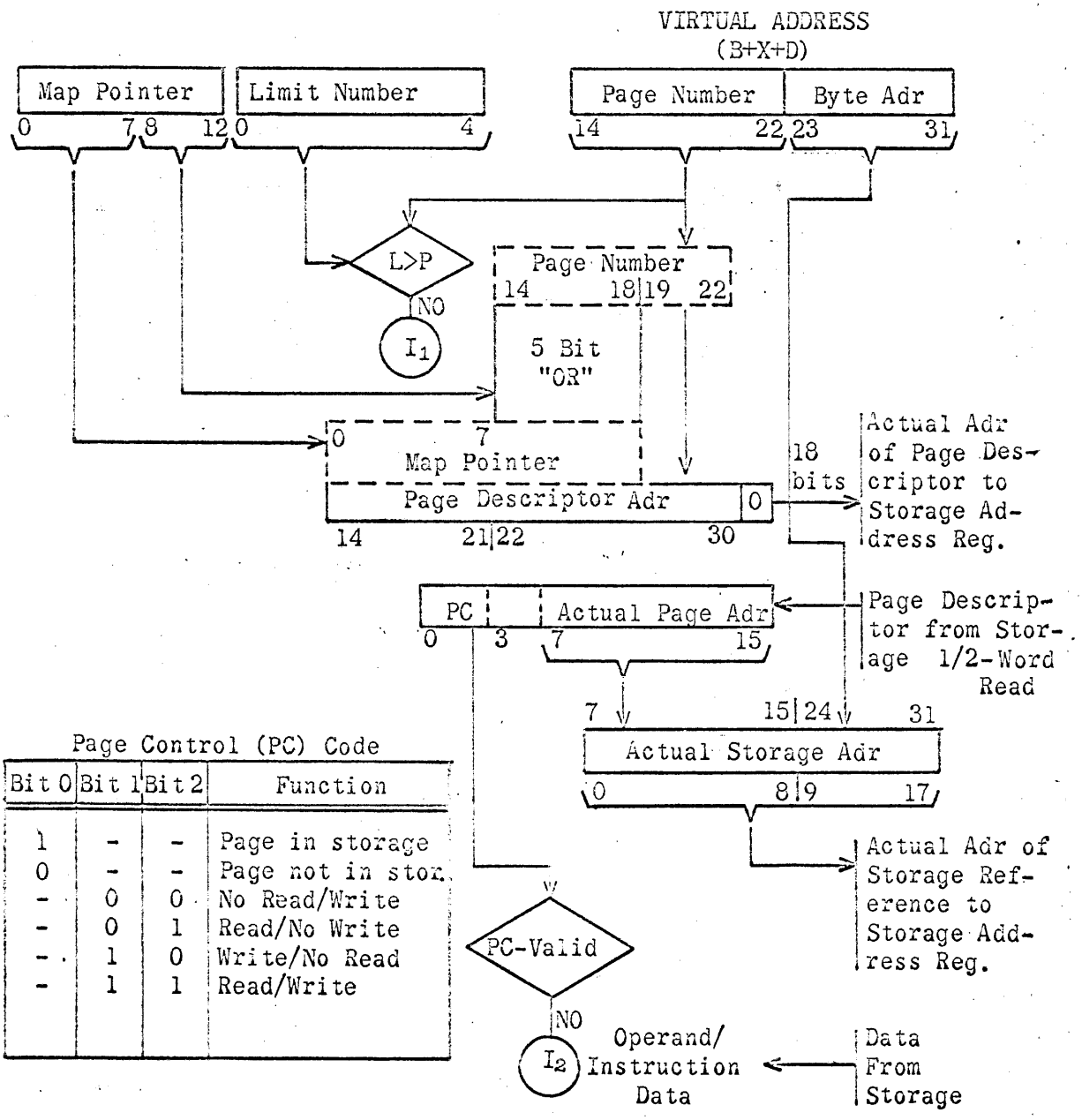

Page Control (PC) Code

Bit 0	Bit 1	Bit 2	Function
1	-	-	Page in storage
0	-	-	Page not in stor.
-	0	0	No Read/Write
-	0	1	Read/No Write
-	1	0	Write/No Read
-	1	1	Read/Write

I_1 INTERRUPT Memory Limit Exception

I_2 INTERRUPT Illegal Reference

Figure 5. Paging Logic

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In order to maintain a high transfer rate on the I/O channels, the address relocation process is performed during I/O access to storage only under the following conditions:

- For first references.
- When a page boundary is crossed.
- For relocation of a Chain Address at the start of each chaining sequence.
- When a transfer-in-channel is processed.

A Limits Check is performed on each access that requires an address relocation translation.

In order to bypass the address relocation process on I/O access to storage the following data must be maintained in the Access Control Register (see Figure 6) for each active I/O device.

- Virtual data page address (data page number)
- Actual data address
- Map pointer
- Limit Number
- Virtual chain address
- Byte count
- Flag information

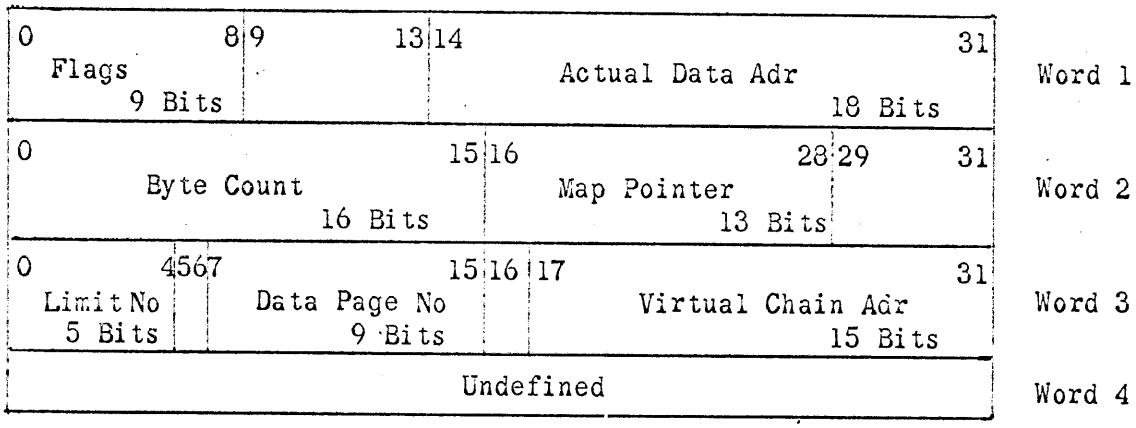


Figure 6. Access Control Register

Note this is not to be confused with the Channel Command Word format which is IBM/360 compatible.

For the Multiplex channel there are 16 bytes allocated in main storage to accommodate the ACR requirements for each of the eight standard subchannels; similarly each communications device, when assigned, has 16 bytes allocated.

2.4.4 Operating and Floating Point Registers

Sixteen full word registers are used for temporary storage of binary operands and/or results. They are used mainly for fixed-point and logical arithmetic and for instruction address indexing. Four double-word registers are used by the floating-point arithmetic instructions. These registers are provided in the form of special integrated flip-flop storage. These registers are addressable only by the special instruction fields provided for their access.

2.5 Operand Addressing

Operands may be found in one of three places. They may be contained within the instruction, stored in either the operating registers or the floating point registers or located in Main Storage. Addressing of operands is not necessary if they are part of the instruction. Addressing is handled by short fields in the instruction when operands are in either of the

register sets. However, when operands are contained in Main Storage, a large address must be formed to obtain them. Formation of this address is explained below.

All instructions which call for operands from Main Storage have one or two Operand Specification Fields and certain instructions have, in addition, an Index Specification (see Figure 7).

X	B	D
4 Bits	4 Bits	12 Bits

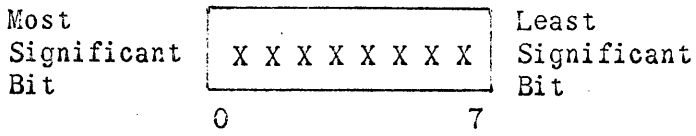
Figure 7. Index and Operand Specification Fields

The displacement (D) is 12 bits long and is used to directly specify a displacement from a selected address base. The base address is found in one of the operating registers which is specified as the base (B). The contents of that register, which is an 18-bit number, is added to the Displacement (D), which is treated as a 12-bit positive number to form the Main Storage address. Certain instructions have, in addition, an index (X) which specifies the operating register that contains the index value. This index value is treated as an 18-bit positive number and is added to the previous sum to determine the Main Storage address. If either the B field or the X field is zero or if both are zero, then zero is added to the address in place of the contents of an operating register. If the displacement is zero, the address is determined by either the base or the index, or both.

2.6 Data Formats

2.6.1 Data Bytes

The 8-bit byte is the basic addressable data unit. The byte can contain a single alpha or numeric character, two decimal digits, a decimal digit and a sign, or a decimal digit and a zone. The byte can also be an 8-bit portion of a fixed or floating point binary number. Two bytes comprise a halfword, four bytes a word, and eight bytes a double word as shown in Figure 8 .



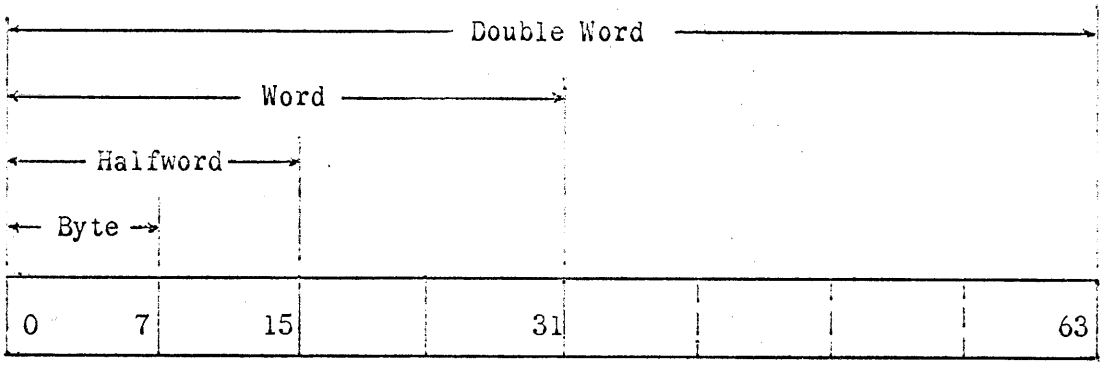


Figure 8. Binary Word Formats

2.6.2 Fixed Point Binary Numbers

All fixed point binary numbers have the same basic format except that they may vary in length. The three basic lengths are shown in Figure 9.

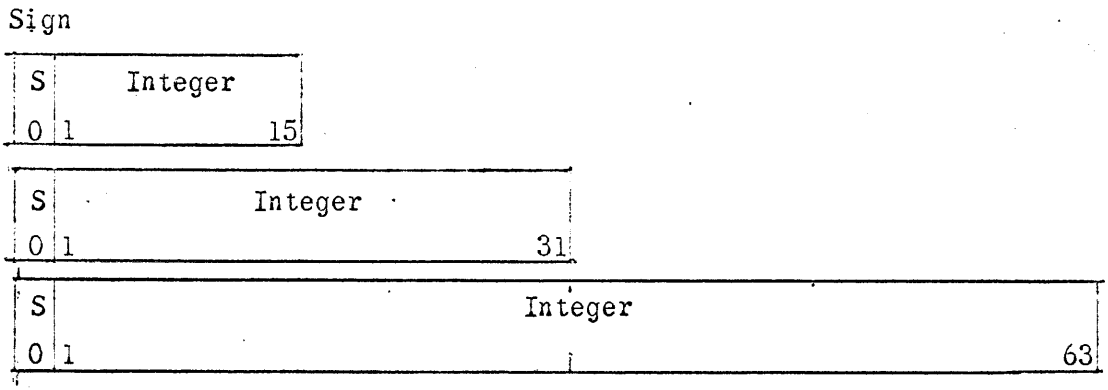


Figure 9. Fixed Point Binary Numbers

Binary numbers are normally called from or stored in Main Storage in one of the first two formats. However, words in the third format may also be stored or retrieved by means of special programming. All three formats are used by the hardware, but the halfword number called from storage will always be expanded to a full word by extending the sign to the left before the arithmetic is performed. Therefore, all fixed point binary arithmetic except the Divide uses full word operands in the actual computation. The Divide instruction calls for a double word as the dividend. The double word is found in an even-odd pair of operating registers. The Multiply instruction forms a double word product which is stored in an even-odd pair of operating registers.

2.6.3 Floating Point Binary Numbers

Floating point binary numbers are of either single or double word size as shown in Figure 10.

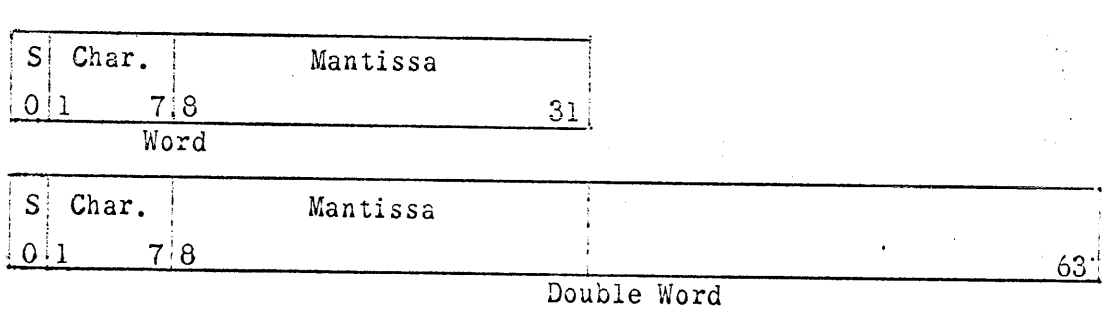


Figure 10. Floating Point Binary Numbers

The first format is that used for single precision floating-point arithmetic while the second is used for double precision floating point operations. Either format may be called from or stored in Main Storage or the floating point registers. All floating point registers are double word registers and their addresses are 0, 2, 4, or 6 in the register specification fields of the instruction.

2.6.4 Decimal Numbers

2.6.4.1 Unpack Decimal Numbers

Figure 11 shows the unpacked decimal format, each byte is divided into two equal fields, a zone field and a digit field. The most significant four bits constitute a zone, and least significant 4 bits the digit. The zone portion of the least significant byte holds the sign of the number.

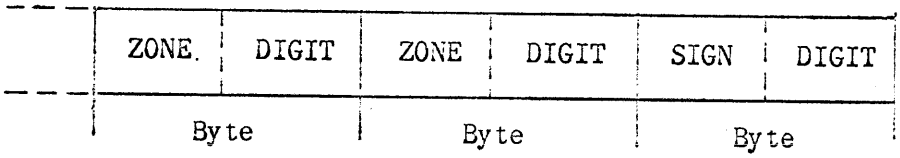


Figure 11. Unpacked Decimal Number Format

2.6.4.2 Packed Decimal Numbers

Figure 12 shows that a packed decimal number contains two digits per byte. The least significant byte holds the sign in the least significant four bits and the least significant digit in the most significant four bits. All decimal arithmetic is performed on packed decimal numbers.

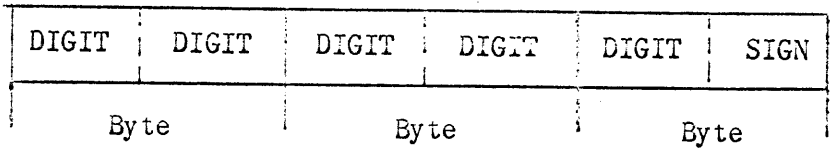


Figure 12. Packed Decimal Number Format

2.7 Program Instructions

The program instructions process fixed length binary numbers in both fixed point and floating point formats, variable length decimal numbers and fixed and variable length logical data; exercise control over processor

operations; and direct peripheral equipment. Five different instruction formats are used: RR (register to register), RX (register to indexed storage and vice versa), RS (register to storage), SI (storage and immediate operand) and SS (storage to storage). The parenthetical expressions refer to operand sources and/or destinations.

2.7.1 Instruction Formats

2.7.1.1 Register to Register (RR) Instruction Format

The RR instructions are two bytes long. The first byte contains the operation code. The second byte contains two 4-bit fields that address either operating or floating point registers. Generally, the first field specifies one operand source and/or the destination of the result. The second field specifies the source of the other operand. The instruction format is shown in Figure 13.

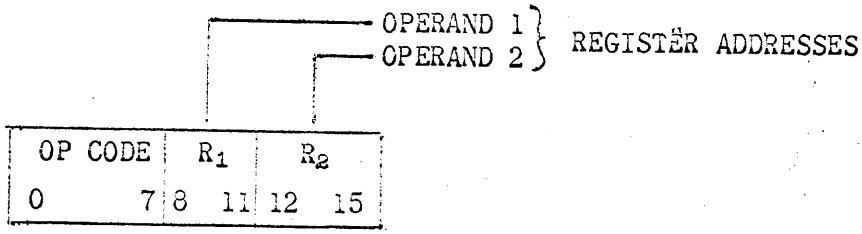


Figure 13. RR Instruction Format

The R_1 field is replaced by an M field which contains a condition mask for the conditional branch instruction.

2.7.1.2 Register to Indexed Storage (RX) Instruction Format

The RX instructions consist of four bytes. The first byte contains the operation code. The second byte consists of two 4-bit fields which specify registers. The first field addresses either an operating or floating point register which is one operand source and/or the result destination. The second field can address operating registers only and specifies a secondary index for determining a storage address. The next two bytes are made up of

a 4-bit field and a 12-bit field. The 12-bit field contains an address displacement by which the contents of the register specified by the 4-bit field is indexed to determine a storage address. The instruction format is shown in Figure 14.

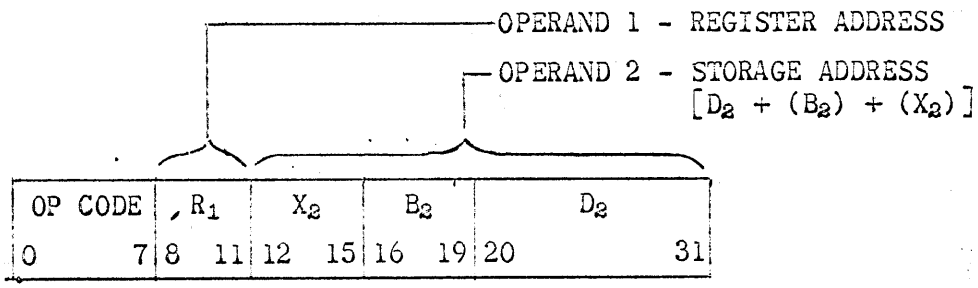


Figure 14. RX Instruction Format

The R_1 field is replaced by an M field which holds a condition mask for the conditional branch instruction.

2.7.1.3 Register to Storage (RS) Instruction Format

The RS instructions are four bytes long as shown in Figure 15. The operation code is contained in the first byte. The first 4-bit field in the second byte specifies an operand and/or a destination for the result. The next 4-bit field specifies a second operand, a limit for multiple register operations or is ignored. The last two bytes in the instruction specify an index register and a displacement value as in the RX format.

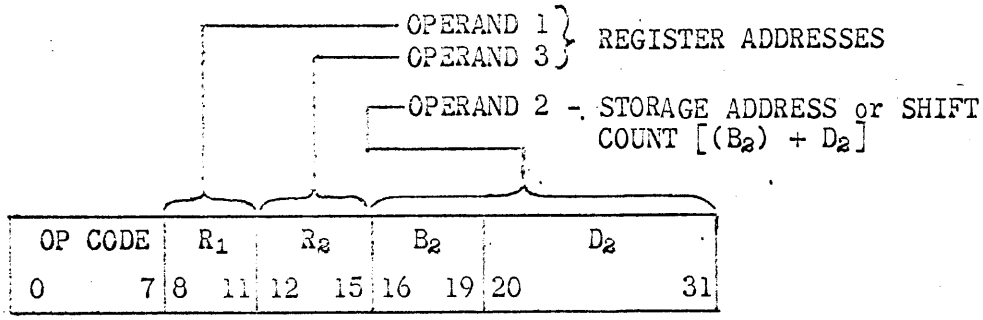


Figure 15. RS Instruction Format

2.7.1.4 Storage and Immediate Operand (SI) Instruction Format

The SI instructions are made of four bytes as shown in Figure 16. As with the other formats, the first byte contains the operation code. The second byte contains an operand which directly enters into the instruction execution. The last two bytes specify an index register and displacement which together determine the address in storage which is the other operand source and/or the result destination.

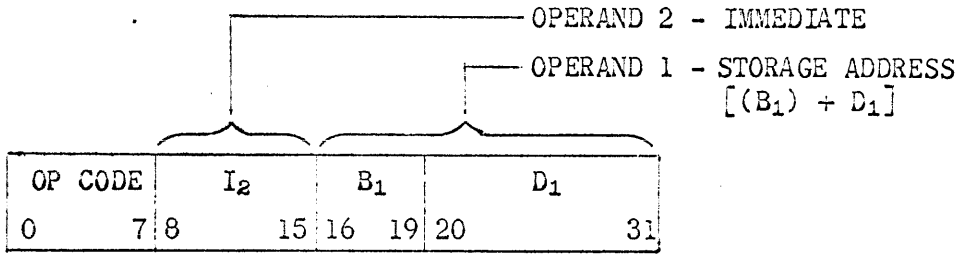


Figure 16. SI Instruction Format

2.7.1.5 Storage to Storage (SS) Instruction Format

The SS instructions are six bytes long as shown in Figure 17. The first byte contains the operation code while the second byte specifies the length (number of bytes) of the operands. For instructions where both operands will always be the same length, the whole byte is used for a single length field. If operands vary in length with respect to each other, the byte is divided into two 4-bit fields, one for each operand. The next two bytes determine the location of the first operand and/or destination while the last two bytes address the second operand. Both address fields are composed of a 12-bit displacement and a 4-bit index specification. Addresses are formed by adding the contents of the index register to the displacement.

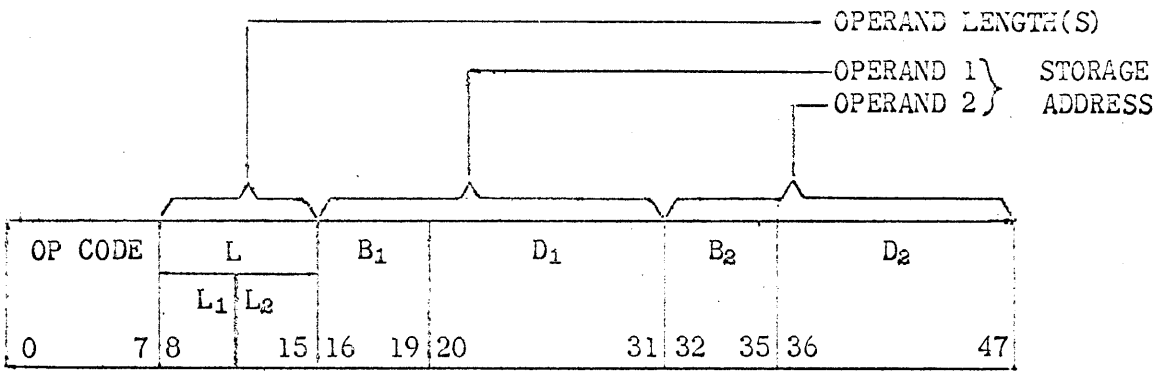


Figure 17. SS Instruction Format

2.7.2 Operation Codes

The 8-bit operation code (OP Code) is expressed by two hexadecimal digits as shown below.

0000 - 0	1000 - 8	0111 - 7
0001 - 1	1001 - 9	1111 - F
0010 - 2	1010 - A	
0011 - 3	1011 - B	
0100 - 4	1100 - C	
0101 - 5	1101 - D	
0110 - 6	1110 - E	

2.7.3 Instruction Repertoire and Timing

The following list of instructions is the repertoire for the 9500 Processor. It is divided into four sections - Supervisor Instructions, Standard Operating Instructions, Floating Point Instructions, and Decimal Instructions. The first two groups of instructions are standard in all machines. The last two groups of instructions are optional and either one or both may be added to any machine.

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The processor cycles per instruction for Standard and Decimal instructions are based on an 18-bit arithmetic section which can add iteratively in a four phase cycle. The processor cyles per floating point instruction are based on the standard 18-bit arithmetic section expanded to 32 bits. This expansion will not affect the number of processor cycles for the standard instructions.

Paging and indexing on operand fetch are included in the processor cycles except that if the operand address crosses a page boundary one cycle must be added to the Load Multiple and Store Multiple instructions. Paging on instruction fetch is included if the boundary is encountered when fetching the first 16 bits of the instruction. If encountered during the second fetch, one extra cycle must be added. The listed cycles reflect the number of minor cycles needed to complete each instruction. To determine the actual time in microseconds, multiply the number of processor cycles by 0.5.

LEGEND

D - number of digit selects and significant starts
R - number of registers loaded/stored
N - number of bytes in result
N_1 - number of bytes in first operand
N_2 - number of bytes in second operand

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SUPERVISOR INSTRUCTIONS

OP Code	Mnemonic	Format	Name	Processor Cycles
9C	SIO	RS	Start I/O	
9E	HIO	RS	Halt I/O	
	SACR	RS	Store Access Control Register	
82	LPSW	SI	Load Program Status Word	
80	SSM	SI	Set System Mask	
	SML	SI	Set Map and Limit	

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STANDARD INSTRUCTIONS

OP Code	Mnemonic	Format	Name	Processor Cycles
04	SPM	RR	Set Program Mask	3
05	BALR	RR	Branch to R2	4
06	BCTR	RR	Branch on Count	4
07	BCR	RR	Branch on Condition	4
0A	SVC	RR	Supervisor Call	
10	LPR	RR	Load Positive	3
11	LNR	RR	Load Negative	3
12	LTR	RR	Load and Test	3
13	LCR	RR	Load and Complement	3
14	NR	RR	And	4
15	CLR	RR	Compare Logical	3
16	OR	RR	Or	4
17	XR	RR	Exclusive Or	3
18	LR	RR	Load	3
19	CR	RR	Compare	3
1A	AR	RR	Add	3
1B	SR	RR	Subtract	3
1C	MR	RR	Multiply	52
1D	DR	RR	Divide	94
1E	ALR	RR	Add Logical	3
1F	SLR	RR	Subtract Logical	3

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OP Code	Mnemonic	Format	Name	Processor Cycles
40	STH	RX	Store Halfword	6
41	LA	RX	Load Address	4
42	STC	RX	Store Character	5
43	IC	RX	Insert Character	5
44	EX	RX	Execute	5
45	BAL	RX	Branch & Link	6
46	BCT	RX	Branch on Count	6
47	BC	RX	Branch on Condition	4
48	LH	RX	Load Halfword	6
49	CH	RX	Compare Halfword	6
4A	AH	RX	Add Halfword	6
4B	SH	RX	Subtract Halfword	6
4C	MH	RX	Multiply Halfword	29
4E	CVD	RX	Convert to Decimal	
4F	CVB	RX	Convert to Binary	
50	ST	RX	Store	6
54	N	RX	And	6
55	CL	RX	Compare Logical	6
56	O	RX	Or	6
57	X	RX	Exclusive Or	6
58	L	RX	Load	6
59	C	RX	Compare	6
5A	A	RX	Add	6

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OP Code	Mnemonic	Format	Name	Processor Cycles
5B	S	RX	Subtract	6
5C	M	RX	Multiply	54
5D	D	RX	Divide	96
5E	AL	RX	Add Logical	6
5F	SL	RX	Subtract Logical	6
86	BXH	RS	Branch on Index High	10
87	BXLE	RS	Branch on Index Low or Equal	10
88	SRL	RS	Shift Right Single Logical	7
89	SLL	RS	Shift Left Single Logical	7
8A	SRA	RS	Shift Right Single	7
8B	SLA	RS	Shift Left Single	7
8C	SRDL	RS	Shift Right Double Logical	11
8D	SLDL	RS	Shift Left Double Logical	11
8E	SLDA	RS	Shift Right Double	11
8F	SLDA	RS	Shift Left Double	11
90	STM	RS	Store Multiple	6+2R
91	TM	SI	Test Under Mask	6
92	MVI	SI	Move	5
94	NI	SI	And	6

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OP Code	Mnemonic	Format	Name	Processor Cycles
95	CLI	SI	Compare Logical	6
96	OI	SI	Or	7
97	XI	SI	Exclusive Or	6
98	LM	RS	Load Multiple	6+3R
D1	MVN	SS	Move Numerics	5+5N
D2	MVC	SS	Move	5+4N
D3	MVZ	SS	Move Zones	5+5N
D4	NC	SS	AND	5+5N
D5	CLC	SS	Compare Logical	5+5N
D6	OC	SS	OR	5+5N
D7	XC	SS	Exclusive OR	5+5N
DC	TR	SS	Translate	5+7N
DD	TRT	SS	Translate and Test	5+7N
F1	MVO	SS	Move with offset	5+6N
F2	PACK	SS	Pack	5+6N
F3	UNPK	SS	Unpack	5+8N

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FLOATING POINT INSTRUCTIONS (OPTIONAL)

OP Code	Mnemonic	Format	Name	Processor Cycles
6A	AD	RX	Add Normalized (Long)	27
2A	ADR	RR	Add Normalized (Long)	24
7A	AE	RX	Add Normalized (Short)	14
3A	AER	RR	Add Normalized (Short)	11
7E	AU	RX	Add Unnormalized (Short)	11
3E	AUR	RR	Add Unnormalized (Short)	8
6E	AW	RX	Add Unnormalized (Long)	20
2E	AWR	RR	Add Unnormalized (Long)	17
69	CD	RX	Compare (Long)	20
29	CDR	RR	Compare (Long)	17
79	CE	RX	Compare (Short)	10
39	CER	RR	Compare (Short)	3
6D	DD	RX	Divide (Long)	150
2D	DDR	RR	Divide (Long)	147
7D	DE	RX	Divide (Short)	30
3D	DER	RR	Divide (Short)	27
24	HDR	RR	Halve (Long)	5
34	HER	RR	Halve (Short)	3
23	LCDR	RR	Load Complement (Long)	5
33	LCER	RR	Load Complement (Short)	3
68	LD	RX	Load (Long)	8
28	LDR	RR	Load (Long)	5
78	LE	RX	Load (Short)	6

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OP Code	Mnemonic	Format	Name	Processor Cycle
38	LER	RR	Load (Short)	3
21	LNDR	RR	Load Negative (Long)	5
31	LNER	RR	Load Negative (Short)	3
30	LPER	RR	Load Positive (Short)	3
22	LTDR	RR	Load and Test (Long)	5
32	LTER	RR	Load and Test (Short)	3
20	LPDR	RR	Load Positive (Long)	5
6C	MD	RX	Multiply (Long)	90
2C	MDR	RR	Multiply (Long)	87
7C	ME	RX	Multiply (Short)	28
3C	MER	RR	Multiply (Short)	25
6B	SD	RX	Subtract Normalized (Long)	27
2B	SDR	RR	Subtract Normalized (Long)	24
7B	SE	RX	Subtract Normalized (Short)	14
3B	SER	RR	Subtract Normalized (Short)	11
60	STD	RX	Store (Long)	8
70	STE	RX	Store (Short)	6
7F	SU	RX	Subtract Unnormalized (Short)	11
3F	SUR	RR	Subtract Unnormalized (Short)	8
6F	SW	RX	Subtract Unnormalized (Long)	20
2F	SWR	RR	Subtract Unnormalized (Long)	17

DECIMAL INSTRUCTIONS (OPTIONAL)

FA	AP	SS	Add Decimal	11+6N
F9	CP	SS	Compare Decimal	9+4N
FD	DP	SS	Divide Decimal	

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OP Code	Mnemonic	Format	Name	Processor Cycle
DE	ED	SS	Edit	5+4N, +4D
DF	EDMK	SS	Edit and Mark	5+4N, +4D
FC	MP	SS	Multiply Decimal	
FB	SP	SS	Subtract Decimal	11+6N
F8	ZAP	SS	Zero and Add	5+4N

2.8 Program Status Word (PSW)

The PSW groups together many diverse functions of the control section into one program alterable register. Located in the PSW register are the following functions.

P Register - This register contains the address of the next sequential instruction to be read from storage. It is incremented each time an instruction is executed unless a branch (jump) is called for or an interrupt is processed.

Program Mask - These bits when cleared will inhibit certain arithmetic error interrupts from occurring.

Condition Code - The code is set to reflect conditions, such as zero, < zero, overflow, etc., which result from the execution of many arithmetic, logical, and test instructions. The code can then be used to control program branching.

Instruction Length Code - The length, in bytes, of the current instruction is recorded here.

State Designator - A single bit signifies whether the processor is operating in the supervisor or probelm state.

2.9 Interrupts

Interrupts in the 9500 processor are divided into several specific classes. This division allows the processor to rapidly change its state due to a general condition requiring special action. Within each interrupt class there are many subclasses with each one identified by the status information in PSW or the Channel Status Table.

Upon recognizing an interrupt condition the processor stores the old PSW and procures a new one. A new PSW is assigned a fixed location in main storage for each of the specific interrupt classes. The interrupt classes are:

Machine check
Supervisor call
Program
Page exception
I/O (communication subchannel)
I/O (standard subchannel)

- Machine Check Interrupt - This interrupt provides a means for recovery from a machine malfunction. Status information is provided to aid subsequent diagnostic action.

- Supervisor Call Interrupt - This interrupt occurs when a supervisor call instruction is executed. Status information in this case provides a link to parameter information in the calling program.

- Program Interrupt - This interrupt occurs as a result of improper specification, or use of instructions or data.

- Page Exception Interrupt - This interrupt occurs when the processor discovers that an instruction or operand to be used is specified in a page which is not allocated in main storage. This condition is defined by a bit in the Page Descriptor word.

- I/O (communication subchannel) Interrupt - This interrupt occurs when a communications subchannel I/O device requires processor response.

- I/O (standard subchannel) Interrupt - This interrupt occurs when a standard subchannel I/O device requires processor response.

The 9500 processor utilizes an automatic tabling mechanism to eliminate queuing and facilitate the handling of I/O interrupts. The limitation of a single Channel Status Word location is eliminated by providing a Channel Status Table Pointer which points to the location where the next I/O interrupt status is to be stored. Thus I/O interrupt status data is automatically tabled and the I/O interface released for use by other devices. Separate Table Pointers are provided for standard subchannels and communications subchannels. Control of the status pointer registers is privileged.

2.10 Fault Detection

2.10.1 Parity Checking

Each 8-bit byte of storage data has an associated bit which is used to obtain odd parity for each byte. This parity bit is checked as data is read from storage and is regenerated when data, altered by processing, is written into storage. Parity is also checked on input data from peripheral devices. Parity will be generated for the data received

from peripheral devices without a parity bit before it is placed in Main Storage. A parity error on data read from Main Storage is considered a peripheral error.

2.10.2 Error Checking

Detection of parity errors and some abnormal processor conditions will cause an interrupt to be generated which, in turn, will cause control to be transferred to a Fixed Storage Location. Abnormal results from arithmetic operations are of interest to the program but are not necessarily errors.

2.11 Simulation Aids

Simulation of other processors will be aided by the extension of the Standard Instruction set to include Load Immediate, Add Immediate, and Permute Instructions. The Permute Instructions allow Storage-To-Register, Register-To-Storage, and Register-To-Register operations with redefinition (mapping) of bit positions during transfer.

The bit-permutation capability eliminates the excessive use of load/shift sequences which are very time consuming. The Load-Add Immediate Instructions allows for fast clearing and incrementation of the general purpose registers.

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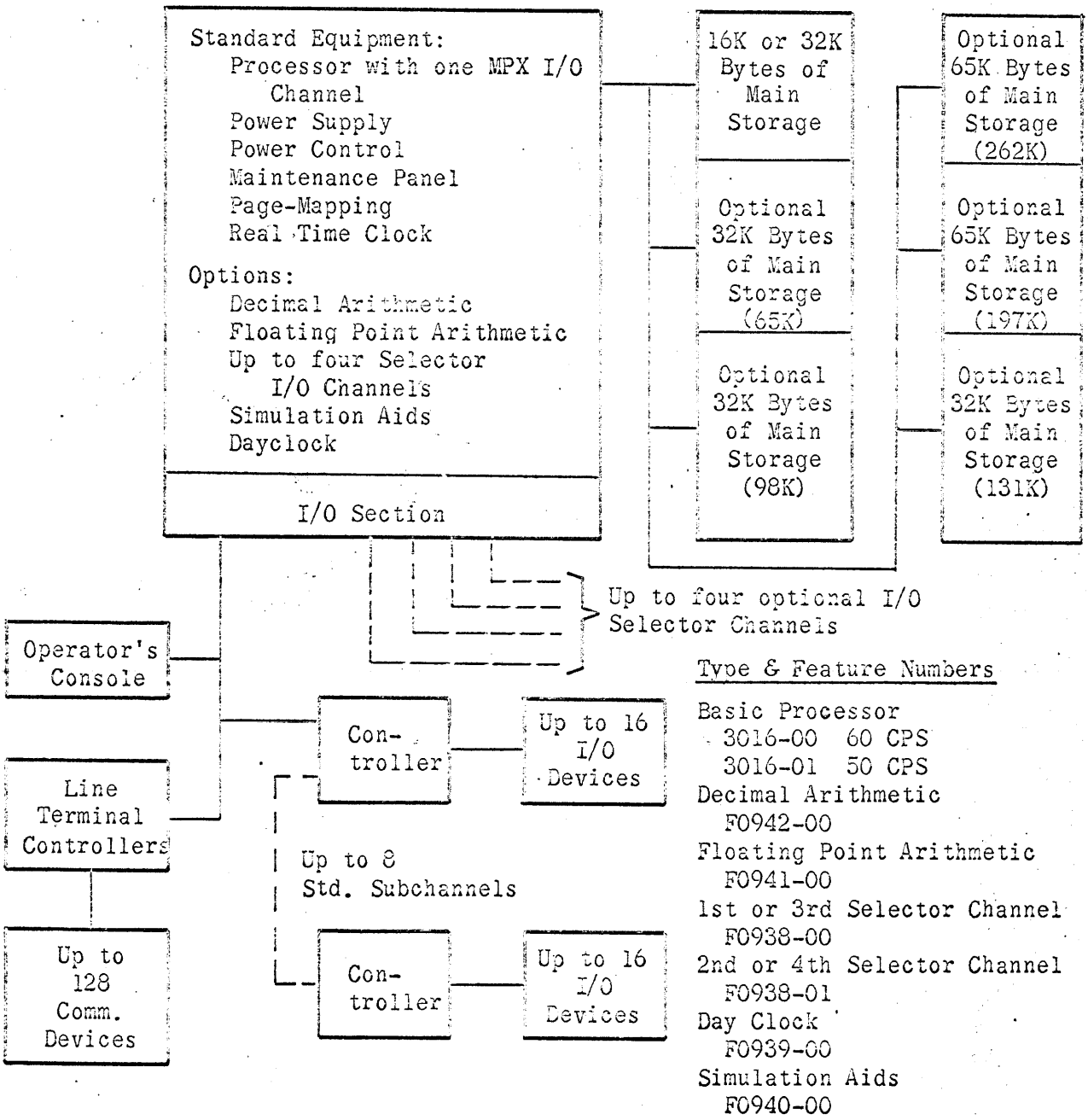
3.0 Configurator



Type & Feature Numbers

Basic Processor
- 3016-00 60 CPS
- 3016-01 50 CPS

Decimal Arithmetic
- F0942-00

Floating Point Arithmetic
- F0941-00

1st or 3rd Selector Channel
- F0938-00

2nd or 4th Selector Channel
- F0938-01

Day Clock
- F0939-00

Simulation Aids
- F0940-00

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3.1 Standard Configuration (without main storage)

The minimum 9500 Processor configuration includes:

- Cabinet with processor, power supply and maintenance panel
- Operators console with desk teletypewriter and keyboard
- One I/O channel (MPX)

See Product Description S-70022 for Main Storage details.

3.2 Optional Features

- 1st I/O channel (Selector)
- 2nd I/O channel (Selector)
- 3rd I/O channel (Selector)
- 4th I/O channel (Selector)
- Dayclock
- Floating Point Arithmetic
- Decimal Arithmetic
- Simulation Aids

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4.0 Operator Controls and Indicators

An Operator's Console will be supplied with the CPU as standard equipment. The console will contain all the controls necessary for the execution of programs and a typewriter-keyboard for operator communication with the CPU. See Operator's Console Product Description S-70023 for details.

A maintenance panel located in the Central Computer cabinet will be provided. This panel will contain the operator bootstrap controls and such trouble shooting aids as rate controls and flip-flop displays. The actual display lights and switches will be mounted on the PC cards which are plugged into the main logic deck.

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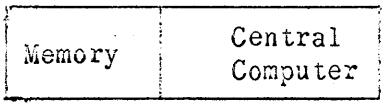
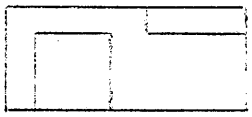
5.0 Physical Characteristics

The UNIVAC 9500 Computer is packaged according to the new UNIVAC Packaging System-II, or UPS-II. The 9500 Computer is composed of a central computer cabinet, a memory cabinet, and an operator's console. Both of these cabinets measure 64 inches in height, 48 inches in width, and 24 inches in depth.

5.1 Installation

Below is a sketch showing a cabinet configuration of the CPU.





Operator's Console

Drawing 4099834 shows the cable access and air intake openings for the central computer cabinet, memory cabinet and operator's console.

The physical characteristics; height, weight, depth, floor loading, and the clearances needed to make each unit accessible for operation and maintenance are as follows:

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Physical Characteristics

	Operator's Console	Central Computer Cabinet	Memory Cabinet
Height	40 in.	64 in.	64 in.
Width	58 in.	48 in.	48 in.
Depth	33 in.	24 in.	24 in.
Weight	300 lbs.	600 lbs.	600 lbs.
Floor Loading	24 lbs./ sq. ft.	75 lbs./ sq. ft.	75 lbs./ sq. ft.
Clearance	72 in. all sides	72 in. front and rear; none to sides	

5.2 Cooling -

Cooling air is drawn into the cabinets either from the false floor or from the room. The heat is exhausted into the room.

Heat Dissipation and Cooling Requirements

	Operator's Console	Central Computer Cabinet	Memory Cabinet
Heat Dissipation (BTU/hr.)	N.A.	7,700	3,400
Cooling Requirements (CFM)	N.A.	940	500 @ 60 CPS 400 @ 50 CPS

5.3 Power

The 9500 processor will be required to use one of the following five power systems, depending on which is available at the particular site. See Environmental Specification P-20050, Revision D.

Input Power Requirements CPU and Memory

System	Voltage	Phase	Freq (CPS)	Service
1.	120/208	1	60	3 Wire
2.	120/240	1	60	3 Wire
3.	220	1	50	2 Wire
4.	230	1	50	2 Wire
5.	240	1	50	2 Wire

5.4 Cables

Cables will enter the cabinets via a false floor; however, provisions for floor raceways will be provided for those installations not able to utilize a false floor. Cables between the Processor and Memory units will be routed within the cabinets.

A cable schedule will be provided.

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6.0 Interface

See Interface Product Specification P-10046.

7.0 Maintainability

The processor will be designed to facilitate "on-call" maintenance and will conform to the general maintainability requirements as stated in the 9500 System Product Description (S-70020).

7.1 Electronic and Logical Considerations

A sufficient amount of indicators, test points and switches will be provided to perform the maintenance functions.

A number of special hardware aids will be provided to aid in malfunction detection and isolation. These will include:

- Flip-flop set and clear capability.
- A phase step mode of operation which will cycle the processor such that the results will be as close as is possible to normal high speed operation.

The equipment shall be designed to necessitate a minimum quantity and variety of field spare parts.

Electrical adjustments shall be such that any number of Field Engineers making the same adjustments can obtain the same result. Adjustments shall be kept to a minimum. A scope may be necessary to perform some adjustments. A scope will be a requirement for maintaining the systems.

7.2 Mechanical Considerations

Regularly scheduled preventive maintenance will not be required. Adjustments will be minimal.

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7.3 Documentation

The following documents should accompany a computer to its site.

- Functional Schematic Diagrams

  Memory Unit
  9500 Processor
  9500 PC Card Schematics

- Maintenance Handbooks

  9500 Processor
  9500 Core Memory
  9500 Operator's Console

- Test Programs

  Command and Arithmetic
  Memory
  Control Register
  Input/Output
  Console

- Shipping Specifications

  Operator's Console
  Central Computer Wired
  Memory Final Assembly

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8.0 Quality

Does not apply.

9.0 Environment

Equipment shall be designed to meet the class B requirements of Equipment Specification, P-20050, Rev. D. Actual Testing under operating conditions shall be performed for temperature, RFI emanation, audible noise, line voltage variations, and for U.L. examination for listing to insure compliance. For other requirements an analytical evaluation shall be required.

The 9500 Processor shall be designed using Emanation Control HGP 0001 and other applicable specifications and standards as design guides. It is not mandatory that this product meet FS222. Design characteristics of FS222 which can be incorporated at no significant increase in cost to the program will be included in the equipment design. The techniques to be implemented, and method of implementation, shall be determined with the guidance of the local Radiation Control Section.

If FS222 compliance is deemed mandatory at a later date a new Product Description and Project Plan is to be initiated.

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Specification completely rewritten and expanded to incorporate current information, e.g. paging mechanism. May 13, 1966.